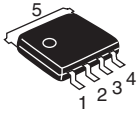


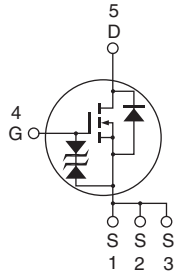
71480E-VB Datasheet

N-Channel 80 V (D-S) MOSFET

PRODUCT SUMMARY			
V _{DS} (V)	R _{DS(on)} (Ω) Max.	I _D (A)	Q _g (Typ.)
80	0.0064 at V _{GS} = 10 V	75 ^a	17.1 nC
	0.0070 at V _{GS} = 6.0 V	65 ^a	
	0.0087 at V _{GS} = 4.5 V	54	



1, 2, 3 Source
4 Gate
5 Drain



FEATURES

- TrenchFET[®] Power MOSFET
- 100 % R_g and UIS Tested

APPLICATIONS

- Primary Side Switching
- Synchronous Rectification
- DC/AC Inverters
- LED Backlighting



RoHS
COMPLIANT
HALOGEN
FREE

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	80	V
Gate-Source Voltage	V _{GS}	± 20	
Continuous Drain Current (T _J = 150 °C)	I _D	T _C = 25 °C	75 ^a
		T _C = 70 °C	62.7
		T _A = 25 °C	28.6 ^{b, c}
		T _A = 70 °C	24.9 ^{b, c}
Pulsed Drain Current (t = 100 μs)	I _{DM}	250	A
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C	
		T _A = 25 °C	4.5 ^{b, c}
Single Pulse Avalanche Current	I _{AS}	30	mJ
Single Pulse Avalanche Energy	E _{AS}	45	
Maximum Power Dissipation	P _D	T _C = 25 °C	120
		T _C = 70 °C	80
		T _A = 25 °C	5 ^{b, c}
		T _A = 70 °C	3.2 ^{b, c}
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150	°C
Soldering Recommendations (Peak Temperature) ^{d, e}		260	

THERMAL RESISTANCE RATINGS				
Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, f}	R _{thJA}	20	25	°C/W
Maximum Junction-to-Case (Drain)	R _{thJC}	1.5	2.0	

Notes

- Package limited.
- Surface mounted on 1" x 1" FR4 board.
- t = 10 s.
- The SOT-669 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under steady state conditions is 70 °C/W.

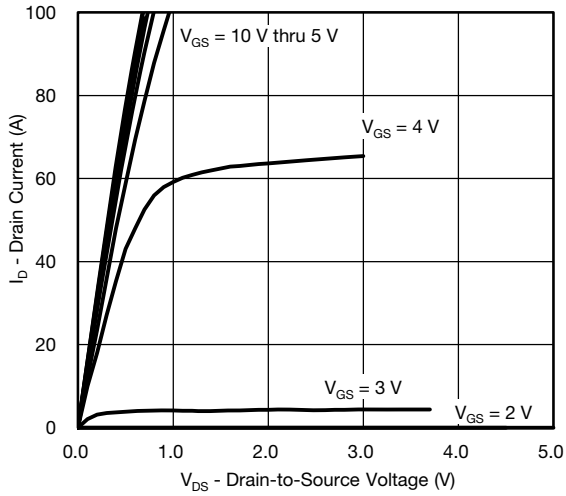
SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	80			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$		37		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			-6.1		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1.4		2.6	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 80\text{ V}, V_{GS} = 0\text{ V}$			1	μA
		$V_{DS} = 80\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	30			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 20\text{ A}$		0.0064		Ω
		$V_{GS} = 6\text{ V}, I_D = 15\text{ A}$		0.0070		
		$V_{GS} = 4.5\text{ V}, I_D = 10\text{ A}$		0.0087		
Forward Transconductance ^a	g_{fs}	$V_{DS} = 10\text{ V}, I_D = 20\text{ A}$		60		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		1855		pF
Output Capacitance	C_{oss}			950		
Reverse Transfer Capacitance	C_{rss}			76		
Total Gate Charge	Q_g	$V_{DS} = 40\text{ V}, V_{GS} = 10\text{ V}, I_D = 10\text{ A}$		35.5	54	nC
		$V_{DS} = 40\text{ V}, V_{GS} = 6\text{ V}, I_D = 10\text{ A}$		22	33	
Gate-Source Charge	Q_{gs}	$V_{DS} = 40\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 10\text{ A}$		17.1	26	
			Gate-Drain Charge	Q_{gd}		
Output Charge	Q_{oss}					
						57
Gate Resistance	R_g		$f = 1\text{ MHz}$	0.5	1.3	2
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 40\text{ V}, R_L = 4\text{ }\Omega$ $I_D \cong 10\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$		12	24	ns
Rise Time	t_r			8	16	
Turn-Off Delay Time	$t_{d(off)}$			32	64	
Fall Time	t_f			7	14	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 40\text{ V}, R_L = 4\text{ }\Omega$ $I_D \cong 10\text{ A}, V_{GEN} = 6.0\text{ V}, R_g = 1\text{ }\Omega$		14	28	
Rise Time	t_r			11	22	
Turn-Off Delay Time	$t_{d(off)}$			30	60	
Fall Time	t_f			8	16	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$			75	A
Pulse Diode Forward Current ($t = 100\text{ }\mu\text{s}$)	I_{SM}				150	
Body Diode Voltage	V_{SD}	$I_S = 5\text{ A}$		0.76	1.1	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 10\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		38	75	ns
Body Diode Reverse Recovery Charge	Q_{rr}			36	70	nC
Reverse Recovery Fall Time	t_a			19		ns
Reverse Recovery Rise Time	t_b			19		

Notes

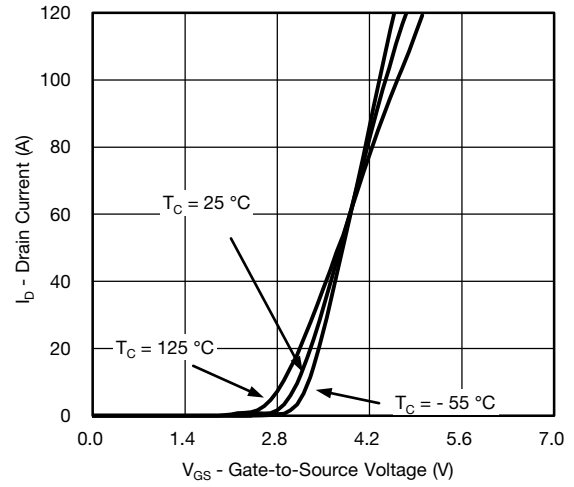
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
 b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

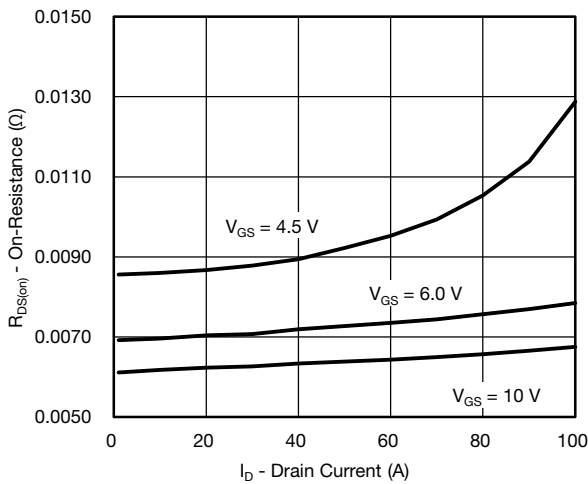
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



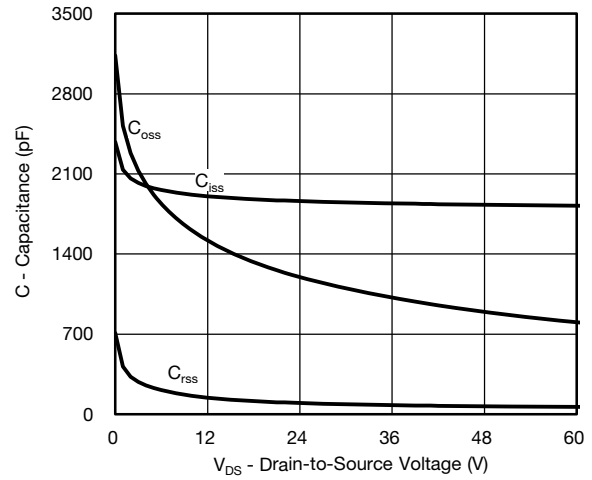
Output Characteristics



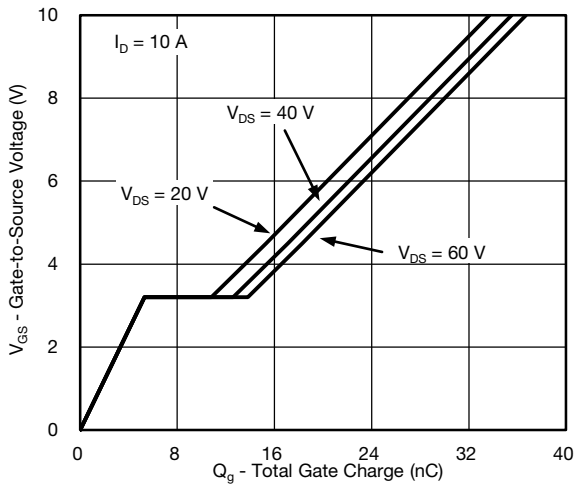
Transfer Characteristics



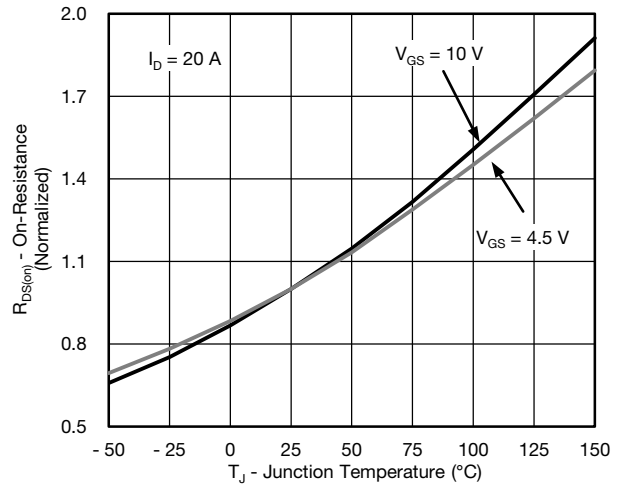
On-Resistance vs. Drain Current



Capacitance

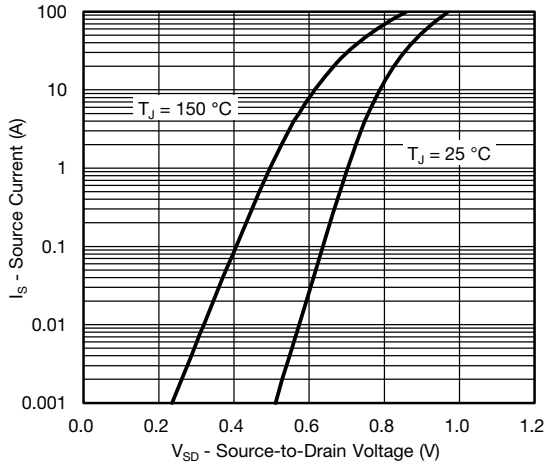


Gate Charge

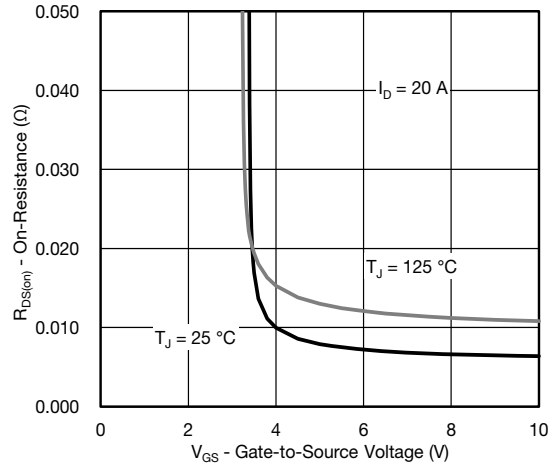


On-Resistance vs. Junction Temperature

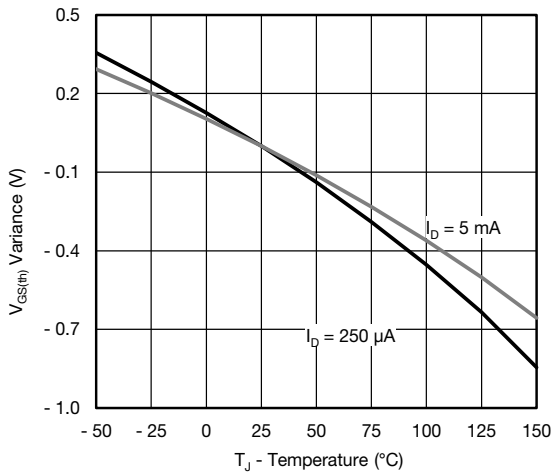
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



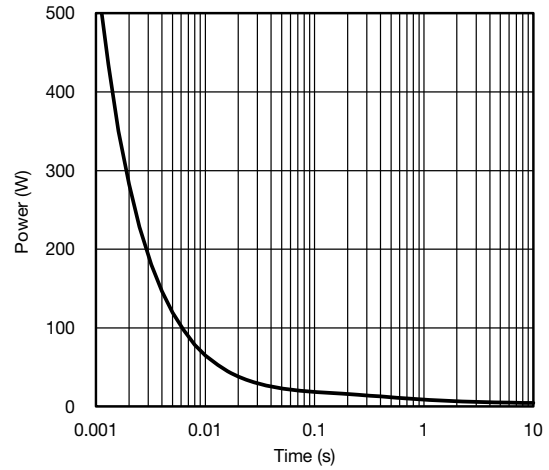
Source-Drain Diode Forward Voltage



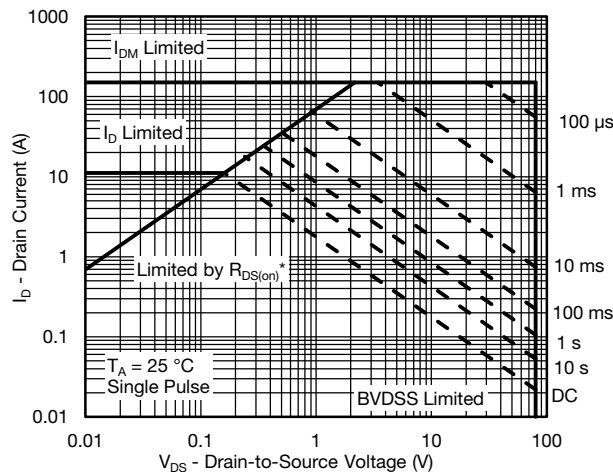
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



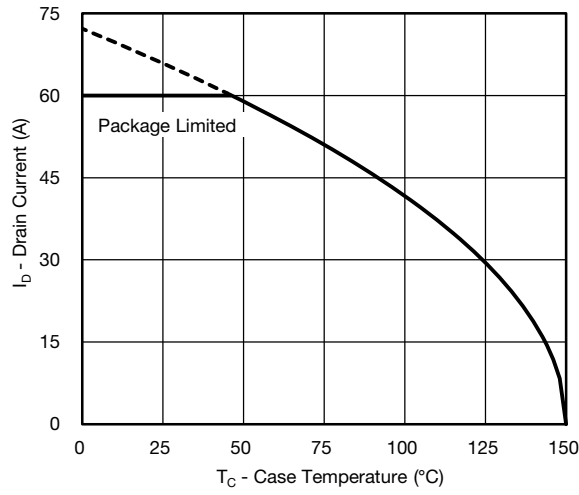
Single Pulse Power, Junction-to-Ambient



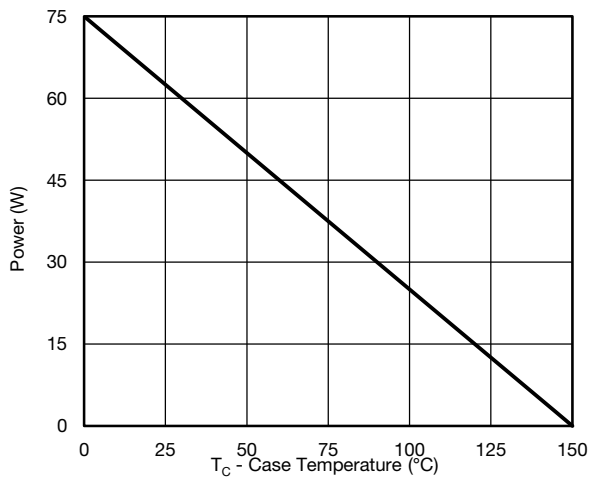
* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

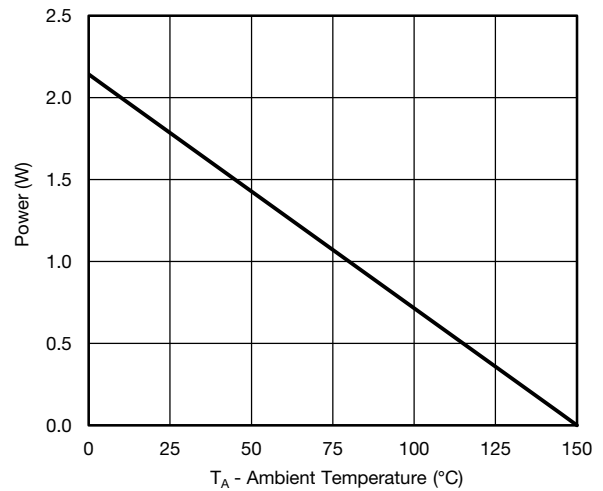
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating*



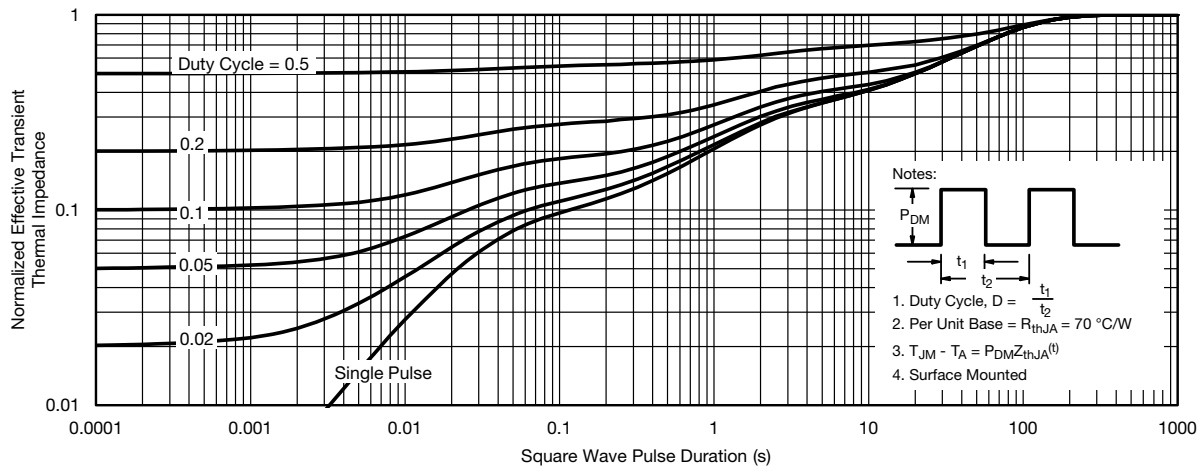
Power, Junction-to-Case



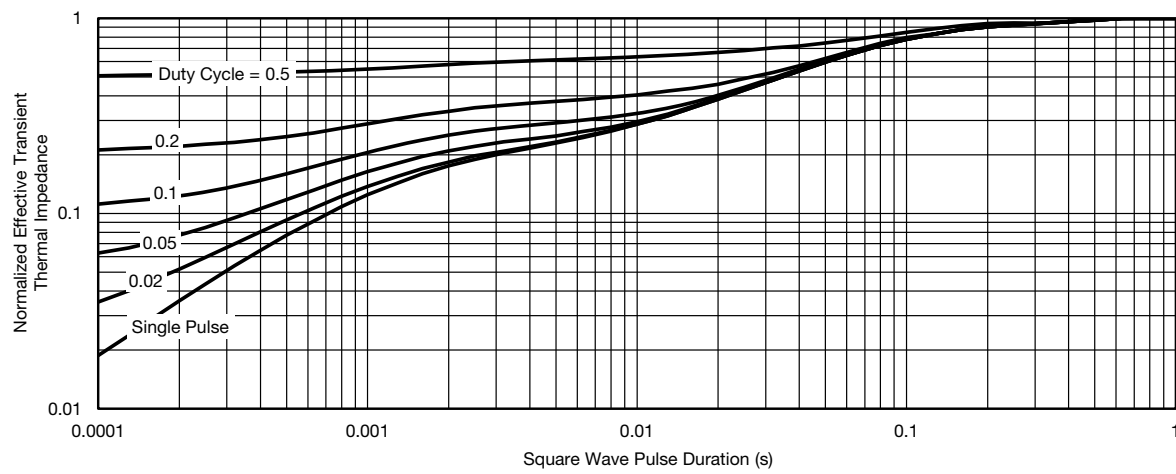
Power, Junction-to-Ambient

* The power dissipation P_D is based on $T_{J(max.)} = 150\text{ }^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

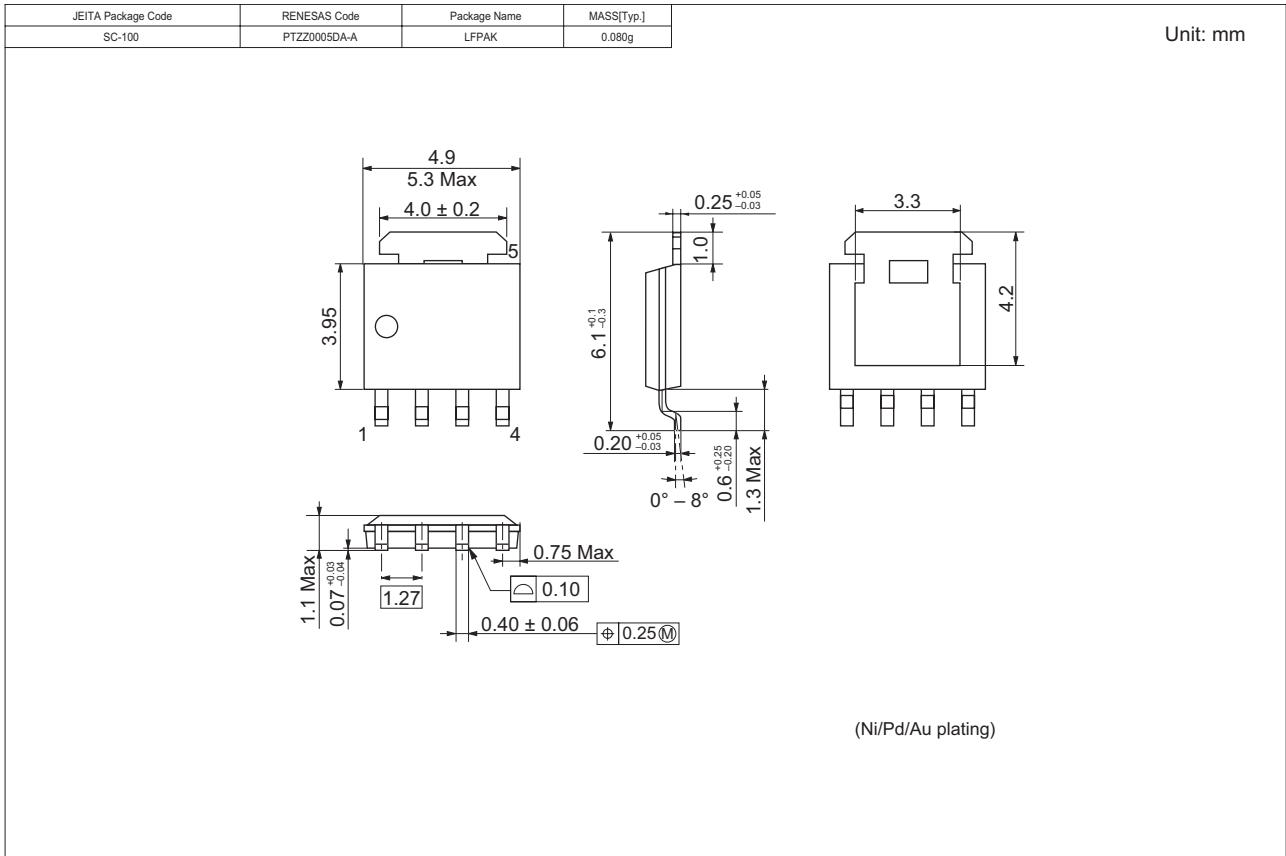


Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

Package Dimensions



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