# LONTIUM SEMICONDUCTOR CORPORATION

ClearEdge™ Technology

# LT8711UXC

# 4-Lane Type-C/DP to HDMI2.0 Converter

# Datasheet

# 1. Features

- **USB Type-C**
  - Compliant with VESA DisplayPort alt mode on USB Type-C standard 1.0
  - Compliant with USB power delivery specification 3.0
  - Compliant with USB Type-C cable and connector specification 1.3
  - Built-in CC controllers for normal communication
  - Support UFP data role
  - Support sink power role
- **DP1.4 Receiver**
  - Compliant with DisplayPort specification 1.4 for 1.62Gbps, 2.7Gbps, 5.4Gbps, 8.1Gbps
  - Compliant Embedded DisplayPort specification version 1.4b
  - Support DisplayPort 1/2/4 lanes
  - Support SSC
  - Support HDCP 1.3/2.3
  - Support HDCP repeater
  - Support 8K@30Hz YCbCr 420 only
  - Support HBE
  - Support HDR10 and Dolby Vision
  - Support ASSR for eDP
  - Support adaptive EQ
- **HDMI2.0 Transmitter**
  - Compliant with HDMI2.0b, HDMI1.4 and DVI1.0
  - Data rate up to 6Gbps
  - Support HDCP 1.4/2.3
  - Support HDCP repeater
  - Support 8K@30Hz YCbCr 420 only
  - Support HDR10 and Dolby Vision
  - Support CEC
  - Programmable transmitter swing and pre-emphasis
- **Miscellaneous**
  - CSC: RGB <-> YUV444 <-> YUV422<-> YUV420
  - Integrated 100/400KHz I2C slave
  - External oscillator 27MHz, +/-50ppm
  - Integrated microprocessor
  - Embedded SPI flash for firmware and HDCP keys
  - Firmware update through I2C/BB interface
  - Power supply: 3.3V for I/O and 1.25V for core

# 2. General Description

The LT8711UXC is a high performance Type-C/DP1.4 to HDMI2.0 converter, designed to connect a USB Type-C source or a DP1.4 source to an HDMI2.0 sink. The LT8711UXC integrates a DP1.4 compliant receiver, and an HDMI2.0 compliant transmitter. Also, a CC controller is included for CC communication to implement DP Alt Mode.

The DP interface comprises 4 main lanes, AUX channel, and HPD signal. The receiver supports maximum 8.1Gbps data rate per lane. The DP receiver incorporates HDCP 1.3/2.3 content protection scheme with embedded key for secure transmission of digital audio-video content.

The HDMI interface includes 4 TMDS clock/data pairs, DDC, and HPD signal. The HDMI transmitter is capable of supporting up to 6Gpbs data rate, quite adequate for handling video resolutions up to UHD 4k 60Hz formats. The HDMI transmitter incorporates HDCP engines which support both HDCP1.4/2.3. With the inclusion of HDCP, the LT8711UXC allows secure transmission of protected content. Embedded key is available that provides the highest level of HDCP key security.

The device is capable of automatic operation which is enabled by an integrated microprocessor that uses an embedded SPI flash for firmware storage. System control is also available through the use of a dedicated configuration I2C slave interface.

# 3. Applications

- Docking station
- Dongle

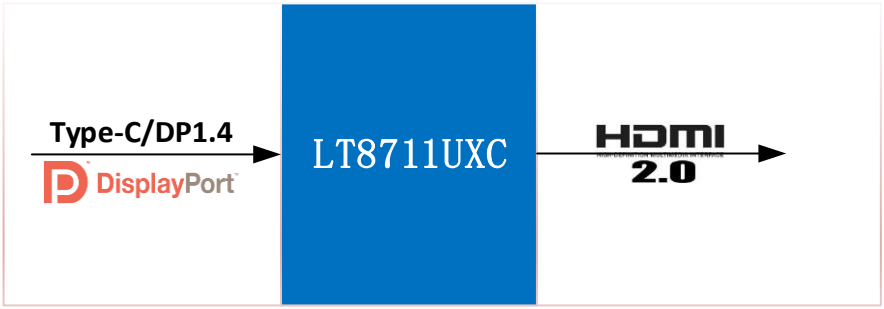


Figure 3.1 Application Diagram

# 4. Ordering Information

Table 4.1 Ordering Information

| Product Name | Part Number | Product Status | Package | Bonding Wire | Grade | Operating Temperature Range | Stack Die Option | Packing Method | MPQ |
|---|---|---|---|---|---|---|---|---|---|
| LT8711UXC | LT8711UXC_U2Q10CED | MP | QFN48 (6*6)Saw | Cu | E | -40℃~85℃ | D | Tray | 4900pcs |

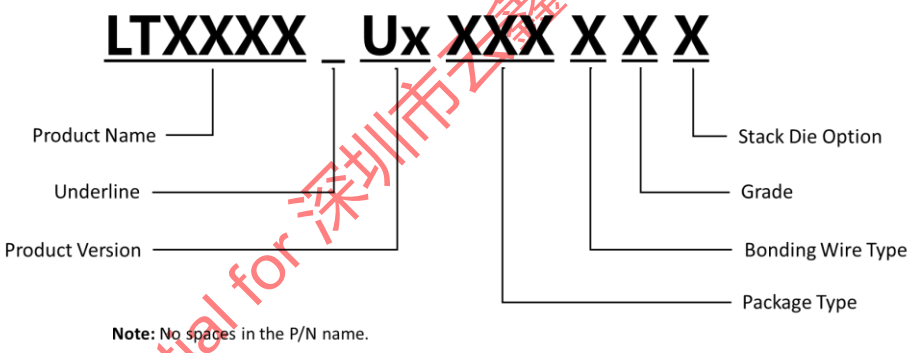


Figure 4.1 Part Number Naming Rules

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# 5. Revision History

| Version | Owner | Content | Date |
|---|---|---|---|
| R1.0 | JX F | Initial U2 Release | 04/04/2023 |
| | | | |
| | | | |

# 6. Pinning Information

## 6.1 Pin Configuration

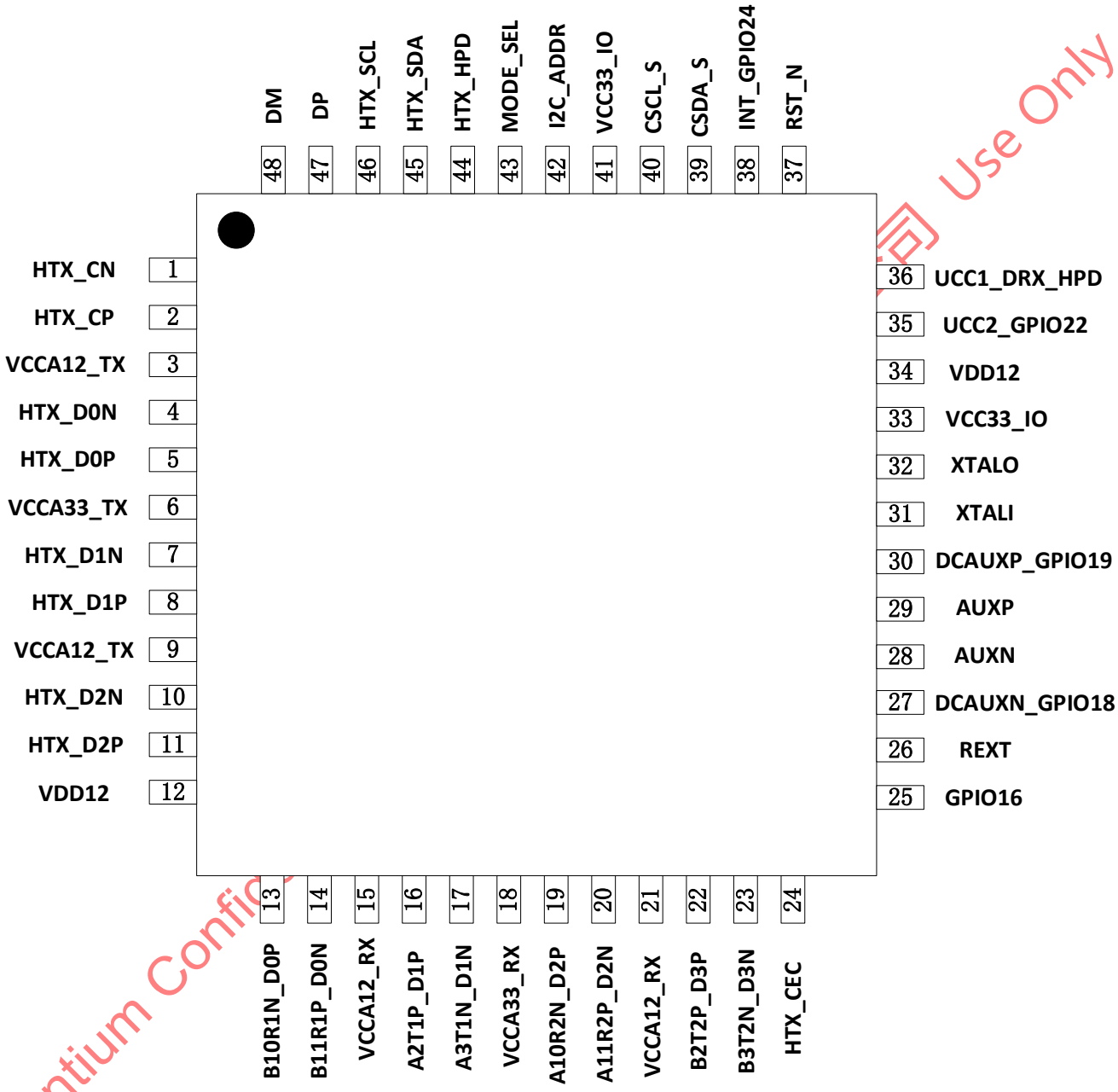





Figure 6.1.1 LT8711UXC QFN48 (6mmx6mm) Pin Assignment (Top View)

## 6.2 Pin Description

**Table 6.2.1 Pin Description**

| PIN# | PIN NAME | I/O TYPE | I/O DIR | DESCRIPTION |
|---|---|---|---|---|
| 1 | HTX_CN | Analog | O | HDMI TX clock channel differential pair negative polarity. |
| 2 | HTX_CP | Analog | O | HDMI TX clock channel differential pair positive polarity. |
| 3 | VCCA12_TX | PWR | I | HDMI TX 1.25V power supply. |
| 4 | HTX_D0N | Analog | O | HDMI TX data0 channel differential pair negative polarity. |
| 5 | HTX_D0P | Analog | O | HDMI TX data0 channel differential pair positive polarity. |
| 6 | VCCA33_TX | PWR | I | HDMI TX 3.3V power supply. |
| 7 | HTX_D1N | Analog | O | HDMI TX data1 channel differential pair negative polarity. |
| 8 | HTX_D1P | Analog | O | HDMI TX data1 channel differential pair positive polarity. |
| 9 | VCCA12_TX | PWR | I | HDMI TX 1.25V power supply. |
| 10 | HTX_D2N | Analog | O | HDMI TX data2 channel differential pair negative polarity. |
| 11 | HTX_D2P | Analog | O | HDMI TX data2 channel differential pair positive polarity. |
| 12 | VDD12 | PWR | I | 1.25V core power supply. |
| 13 | B10R1N_D0P | Analog | I | Type-C High Speed differential pair negative polarity. Positive polarity for DP RX. |
| 14 | B11R1P_D0N | Analog | I | Type-C High Speed differential pair positive polarity. Negative polarity for DP RX. |
| 15 | VCCA12_RX | PWR | I | Type-C/DP RX 1.25V power supply. |
| 16 | A2T1P_D1P | Analog | I | Type-C High Speed differential pair positive polarity. Positive polarity for DP RX. |
| 17 | A3T1N_D1N | Analog | I | Type-C High Speed differential pair negative polarity. Negative polarity for DP RX. |
| 18 | VCCA33_RX | PWR | I | Type-C/DP RX 3.3V power supply. |
| 19 | A10R2N_D2P | Analog | I | Type-C High Speed differential pair negative polarity. Positive polarity for DP RX. |
| 20 | A11R2P_D2N | Analog | I | Type-C High Speed differential pair positive polarity. Negative polarity for DP RX. |
| 21 | VCCA12_RX | PWR | I | Type-C/DP RX 1.25V power supply. |
| 22 | B2T2P_D3P | Analog | I | Type-C High Speed differential pair positive polarity. Positive polarity for DP RX. |
| 23 | B3T2N_D3N | Analog | I | Type-C High Speed differential pair negative polarity. Negative polarity for DP RX. |
| 24 | HTX_CEC | LVTTL OD | I/O | HDMI CEC IO. 3.3V tolerance. |

| PIN# | PIN NAME | I/O TYPE | I/O DIR | DESCRIPTION |
|---|---|---|---|---|
| 25 | GPIO16 | LVTTL | I/O | General Purpose I/O. 3.3V tolerance. |
| 26 | REXT | Analog | O | Bandgap external resistor for current reference. Connect 12k (1%) resistor to ground. |
| 27 | DCAUXN_GPIO18 | LVTTL | I/O | DP AUX DC detect negative polarity (DC-coupled). It also can be configured as General Purpose I/O. 3.3V tolerance. |
| 28 | AUXN | Analog | I/O | DP AUX differential pair negative polarity (AC-coupled). |
| 29 | AUXP | Analog | I/O | DP AUX differential pair positive polarity (AC-coupled). |
| 30 | DCAUXP_GPIO19 | LVTTL | I/O | DP AUX DC detect positive polarity (DC-coupled). It also can be configured as General Purpose I/O. 3.3V tolerance. |
| 31 | XTALI | Analog | I | Crystal oscillator interface input. |
| 32 | XTALO | Analog | I/O | Crystal oscillator interface input/output. |
| 33 | VCC33_IO | PWR | I | 3.3V IO power supply. |
| 34 | VDD12 | PWR | I | Digital core 1.25V power supply. |
| 35 | UCC2_GPIO22 | Analog LVTTL | I/O | CC2 pin for upstream USB Type-C port. It also can be configured as General Purpose I/O. 5V tolerance. |
| 36 | UCC1_DRX_HPD | Analog LVTTL | I/O | CC1 pin for upstream USB Type-C port. It also can be configured as HPD of DP RX. 5V tolerance. |
| 37 | RST_N | LVTTL | I | Hardware reset pin, active low. Connect a resistor pullup to 3.3V power and a cap connected to ground to this pin. |
| 38 | INT_GPIO24 | LVTTL | I/O | Interrupt I/O. It also can be configured as General Purpose I/O. 3.3V tolerance. |
| 39 | CSDA_S | LVTTL OD | I/O | Configuration slave I2C interface. 5V tolerance. |
| 40 | CSCL_S | LVTTL OD | I | Configuration slave I2C interface. 5V tolerance. |
| 41 | VCC33_IO | PWR | I | 3.3V IO power supply. |
| 42 | I2C_ADDR | LVTTL Analog | I/O | I2C address select pin. It also can be configured as General Purpose I/O. 3.3V tolerance. |
| 43 | MODE_SEL | LVTTL Analog | I/O | Chip mode select pin. It also can be configured as General Purpose I/O. 3.3V tolerance. |
| 44 | HTX_HPD | LVTTL | I | HPD input of HDMI TX. 5V tolerance. |
| 45 | HTX_SDA | LVTTL OPD | I/O | DDC interface of HDMI TX. 5V tolerance. |
| 46 | HTX_SCL | LVTTL OPD | I/O | DDC interface of HDMI TX. 5V tolerance. |
| 47 | DP | Analog | I/O | BB PHY interface. |
| 48 | DM | Analog | I/O | BB PHY interface. |
| 49 | EPAD | GND | | |

# 7. Function Description

## 7.1 Function Block Diagram

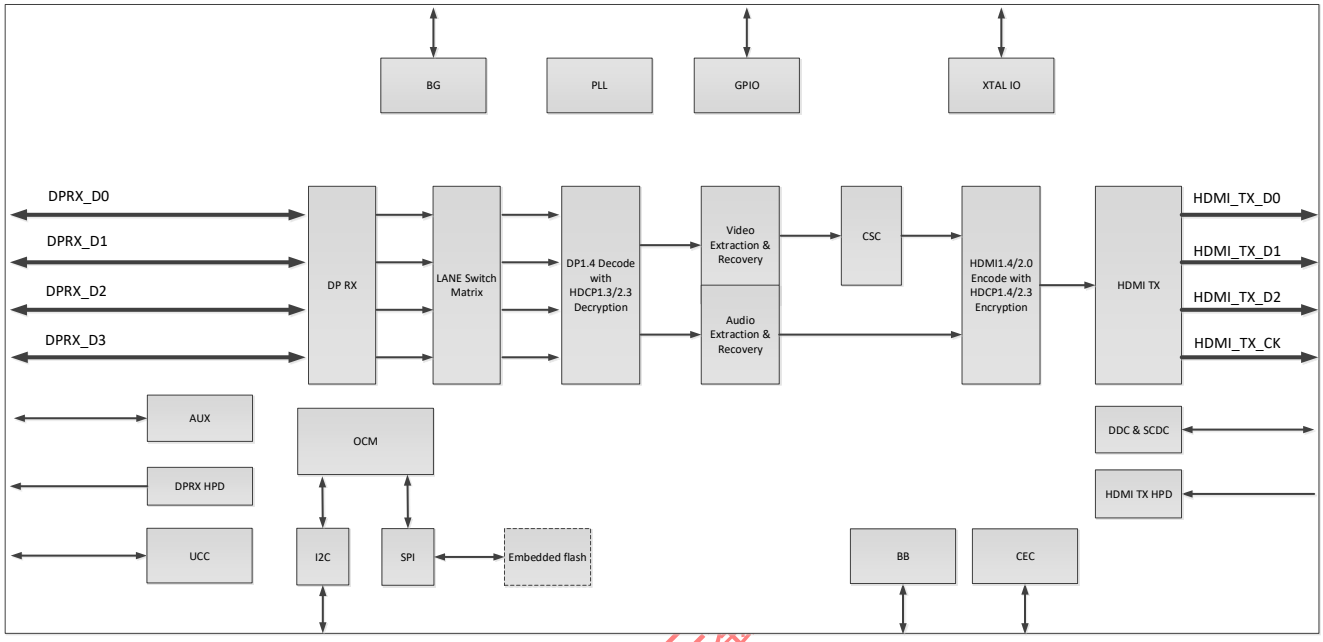



**Figure 7.1.1 Function Block Diagram**

# 8. Specification

## 8.1 Absolute Maximum Conditions

**Table 8.1.1 Absolute Maximum Conditions**

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| VCCA33_TX, VCC33_TX, VCCA33_RX, VCC33_IO | 3.3V Power Supply Voltage | -0.3 | | 4.0 | V |
| VCCA12_RX, VCCA12_TX, VDD12 | 1.25V Power Supply Voltage | -0.3 | | 1.5 | V |
| $V_I$ / $V_O$ | CMOS Terminal Input/Output Voltage Range | -0.3 | | VCC33_IO + 0.3 | V |
| $V_{I(5V)}$ / $V_{O(5V)}$ | 5V Tolerant Input/Output Voltage Range | -0.3 | | 6 | V |
| $T_S$ | Storage Temperature | -65 | | 150 | ℃ |
| $T_J$ | Junction Temperature | | | 125 | ℃ |
| ESD | HBM | | TBD | | V |
| | CDM | | TBD | | V |
| **Note:** Permanent device damage may occur if absolute maximum conditions are exceeded. | | | | | |

## 8.2 Normal Operating Conditions

**Table 8.2.1 Normal Operating Conditions**

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| VCCA33_TX, VCCA33_RX, VCC33_IO | 3.3V Power Supply Voltage | 2.97 | 3.3 | 3.63 | V |
| VCCA12_RX, VCCA12_TX, VDD12 | 1.25V Power Supply Voltage | 1.2 | 1.25 | 1.32 | V |
| $T_A$ | Operating Free-air Temperature | -40 | | 85 | ℃ |
| $\theta_{JC}$ | Junction to Case Thermal Resistance | | 14.27 | | ℃/W |

## 8.3 DC Characteristics

**Table 8.3.1 DC Characteristics**

| DP Main Link Receiver | | | | | |
|---|---|---|---|---|---|
| **Parameter** | **Condition** | **Min** | **Typ** | **Max** | **Units** |
| Unit Interval | HBR3 | | 123 | | ps |
| Unit Interval | HBR2 | | 185 | | ps |
| Unit Interval | HBR | | 370 | | ps |
| Unit Interval | RBR | | 617 | | ps |
| SSC Down-spreading | | 0 | | 0.5 | % |
| SSC Modulation Frequency | | 30 | | 33 | kHz |

| | | | | | |
|---|---|---|---|---|---|
| Differential Eye Voltage | at input pins | 100 | | 1320 | mVp-p |
| **DP AUX Channel** | | | | | |
| **Parameter** | **Condition** | **Min** | **Typ** | **Max** | **Units** |
| Unit Interval | | 0.4 | 0.5 | 0.6 | us |
| Differential Voltage | Transmitting | 390 | | 1380 | mVp-p |
| Differential Voltage | Receiving | 320 | | 1360 | mVp-p |
| AC-Coupling Capacitor | | 75 | | 200 | nF |
| **HDMI Transmitter** | | | | | |
| **Parameter** | **Condition** | **Min** | **Typ** | **Max** | **Units** |
| Single-ended High Level Output Voltage | HDMI1.4 | VCCA33_TX-200 | | VCCA33_TX+10 | mV |
| | HDMI2.0 data channel | VCCA33_TX-400 | | VCCA33_TX+10 | mV |
| | HDMI2.0 clock channel | VCCA33_TX-400 | | VCCA33_TX+10 | mV |
| Single-ended Low Level Output Voltage | HDMI1.4 | VCCA33_TX-700 | | VCCA33_TX-400 | mV |
| | HDMI2.0 data channel | VCCA33_TX-1000 | | VCCA33_TX-400 | mV |
| | HDMI2.0 clock channel | VCCA33_TX-1000 | | VCCA33_TX-200 | mV |
| Single-ended Output Swing Voltage | HDMI1.4 | 400 | | 600 | mV |
| | HDMI2.0 data channel | 400 | | 600 | mV |
| | HDMI2.0 clock channel | 200 | | 600 | mV |

**Table 8.3.2 I2C ADDR select**

| input voltage recommended(V) | Threshold voltage（V） | Output code | I2C address |
|---|---|---|---|
| 0.25 | 0.5 | 000 | 0X52 |
| 0.7 | 0.9 | 001 | 0X56 |
| 1.1 | 1.3 | 010 | 0X5A |
| 1.5 | 1.7 | 011 | 0X5E |
| 1.9 | 2.1 | 100 | 0X72 |
| 2.3 | 2.5 | 101 | 0X76 |
| 2.7 | 2.9 | 110 | 0X7A |
| >3 | | 111 | 0X7E |

## 8.4 AC Characteristics

**Table 8.4.1 AC Characteristics**

| **DP Main Link Receiver** | | | | | |
|---|---|---|---|---|---|
| **Parameter** | **Condition** | **Min** | **Typ** | **Max** | **Units** |

| | | | | | |
|---|---|---|---|---|---|
| Lane intra-pair skew tolerance | For HBR3 | | | 50 | ps |
| | For HBR2 | | | 50 | ps |
| | For HBR | | | 60 | ps |
| | For RBR | | | 260 | ps |
| Jitter closed-loop tracking bandwidth | For HBR3 | 15 | | | MHz |
| | For HBR2 | 10 | | | MHz |
| | For HBR | 10 | | | MHz |
| | For RBR | 5.4 | | | MHz |
| **TMDS TX AC Specifications** | | | | | |
| **Parameter** | **Condition** | **Min** | **Typ** | **Max** | **Units** |
| Rise/Fall Time (20%-80%) | HDMI1.4 | 75 | | | ps |
| | HDMI2.0 data channel | 42.5 | | | ps |
| | HDMI2.0 clock channel | 75 | | | ps |
| Intra-pair Skew | | | | 0.15 | $T_{bit}$ |
| Inter-pair Skew | | | | 0.2 | $T_{character}$ |
| Clock Duty Cycle | | 40% | | 60% | |
| TMDS Clock Jitter | HDMI1.4 | | | 0.25 | $T_{bit}$ |
| | HDMI2.0 | | | 0.3 | $T_{bit}$ |
| Maximum Differential Voltage | HDMI2.0 | | | 780 | mV |
| Minimum Differential Voltage | HDMI2.0 | -780 | | | mV |

## 8.5 Power Consumption

**Table 8.5.1 Power Consumption**

| Condition | | Supply Current (3.3V) | Supply Current (1.25V) | Unit |
|---|---|---|---|---|
| 8K@30Hz | 4Lane@8.1G | 58 | 668 | mA |
| 4K@60Hz | 2Lane@8.1G | 58 | 593 | mA |
| | 4Lane@5.4G | 49 | 489 | mA |
| 4K@30Hz | 2Lane@5.4G | 43 | 379 | mA |
| | 4Lane@2.7G | 35 | 278 | mA |
| 1080P@60Hz | 1Lane@5.4G | 42 | 324 | mA |
| | 2Lane@2.7G | 34 | 229 | mA |
| | 4Lane@1.62G | 42 | 174 | mA |

## 8.6 Power-up Sequence

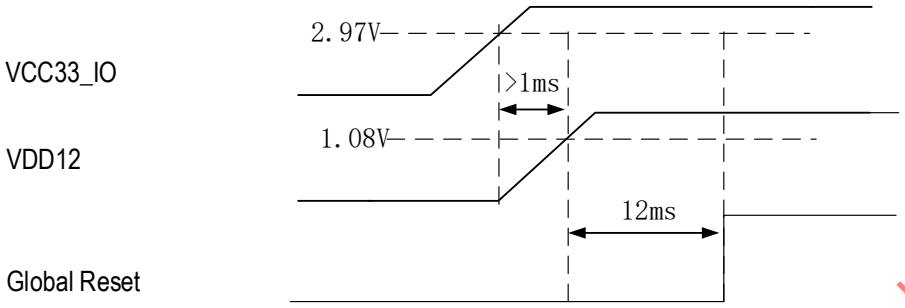
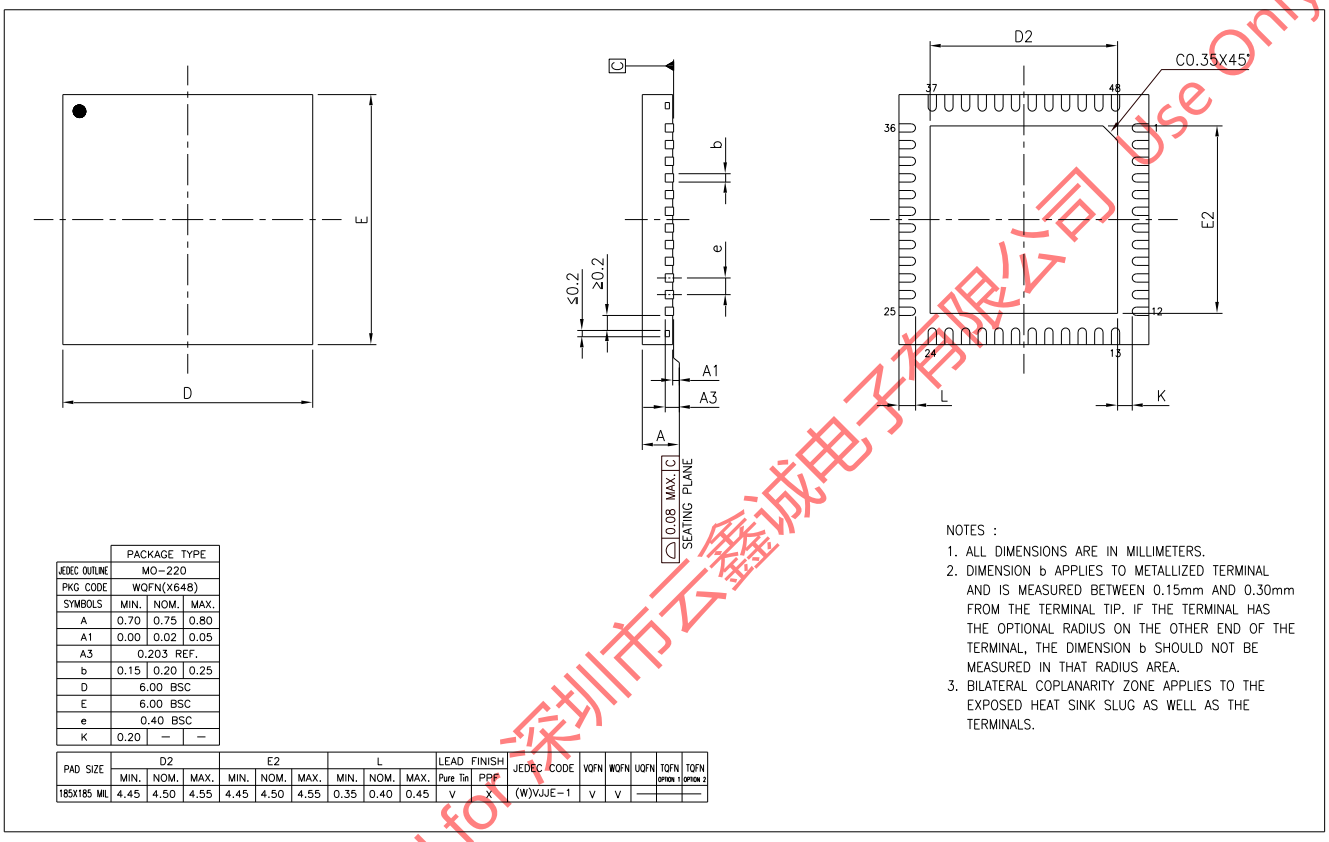



**Figure 8.6.1 Power-up Sequence**

# 9. Package Information

## 9.1 Package Dimensions

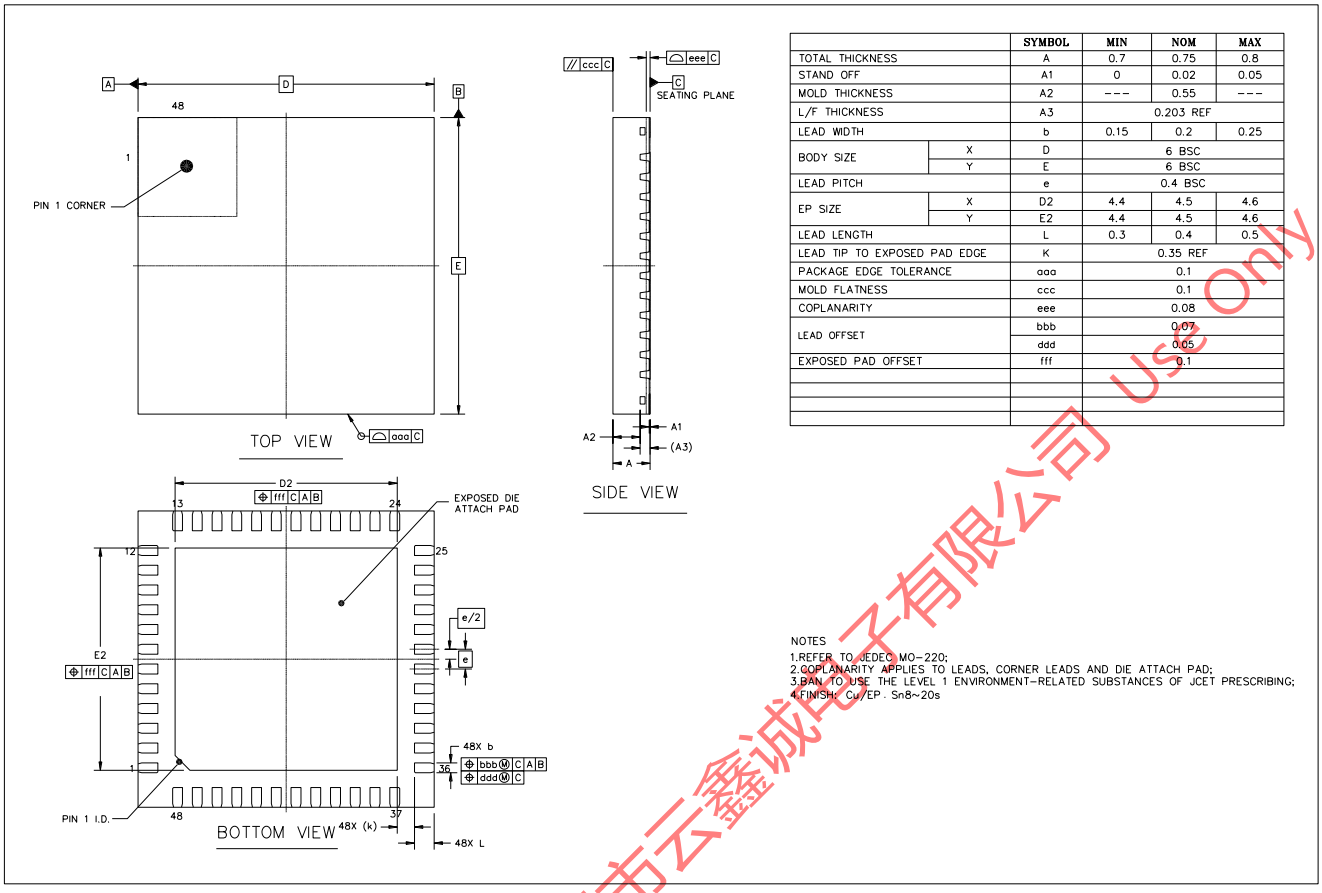
Figure 9.1.1 is the package dimensions for the date code beginning with GT.
Figure 9.1.2 is the package dimensions for the date code beginning with JC.




| | PACKAGE TYPE | | |
|---|---|---|---|
| JEDEC OUTLINE | MO-220 | | |
| PKG CODE | WQFN(X648) | | |
| SYMBOLS | MIN. | NOM. | MAX. |
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0.00 | 0.02 | 0.05 |
| A3 | 0.203 REF. | | |
| b | 0.15 | 0.20 | 0.25 |
| D | 6.00 BSC | | |
| E | 6.00 BSC | | |
| e | 0.40 BSC | | |
| K | 0.20 | — | — |

| PAD SIZE | D2 | | | E2 | | | L | | | LEAD FINISH | | JEDEC CODE | VQFN | WQFN | UQFN | TQFN OPTION 1 | TQFN OPTION 2 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. | Pure Tin | PPF | | | | | | |
| 185X185 MIL | 4.45 | 4.50 | 4.55 | 4.45 | 4.50 | 4.55 | 0.35 | 0.40 | 0.45 | V | X | (W)VJJE-1 | V | V | | | |

**Figure 9.1.1 Package Dimensions (GT)**




| | | SYMBOL | MIN | NOM | MAX |
|---|---|---|---|---|---|
| TOTAL THICKNESS | | A | 0.7 | 0.75 | 0.8 |
| STAND OFF | | A1 | 0 | 0.02 | 0.05 |
| MOLD THICKNESS | | A2 | --- | 0.55 | --- |
| L/F THICKNESS | | A3 | | 0.203 REF | |
| LEAD WIDTH | | b | 0.15 | 0.2 | 0.25 |
| BODY SIZE | X | D | | 6 BSC | |
| | Y | E | | 6 BSC | |
| LEAD PITCH | | e | | 0.4 BSC | |
| EP SIZE | X | D2 | 4.4 | 4.5 | 4.6 |
| | Y | E2 | 4.4 | 4.5 | 4.6 |
| LEAD LENGTH | | L | 0.3 | 0.4 | 0.5 |
| LEAD TIP TO EXPOSED PAD EDGE | | K | | 0.35 REF | |
| PACKAGE EDGE TOLERANCE | | aaa | | 0.1 | |
| MOLD FLATNESS | | ccc | | 0.1 | |
| COPLANARITY | | eee | | 0.08 | |
| LEAD OFFSET | | bbb | | 0.07 | |
| | | ddd | | 0.05 | |
| EXPOSED PAD OFFSET | | fff | | 0.1 | |

NOTES
1.REFER TO JEDEC MO-220;
2.COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD;
3.BAN TO USE THE LEVEL 1 ENVIRONMENT-RELATED SUBSTANCES OF JCET PRESCRIBING;
4.FINISH: Cu/EP . Sn8~20s

**Figure 9.1.2 Package Dimensions (JC)**

## 9.2 Packing Dimensions

Figure 9.2.1 is the packing dimensions for the date code beginning with GT.
Figure 9.2.2 is the packing dimensions for the date code beginning with JC.

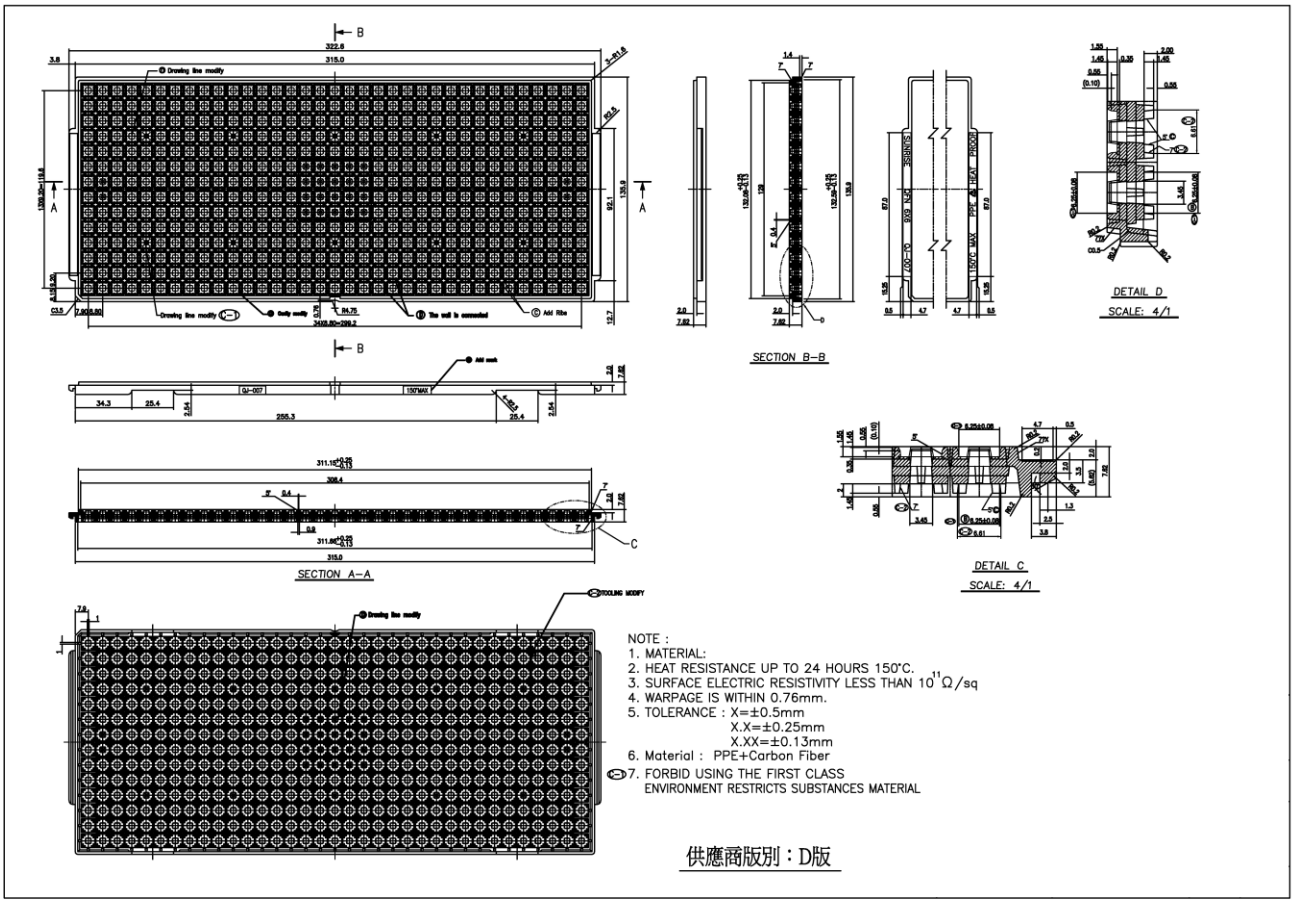



**Figure 9.2.1 Packing Dimensions (GT)**

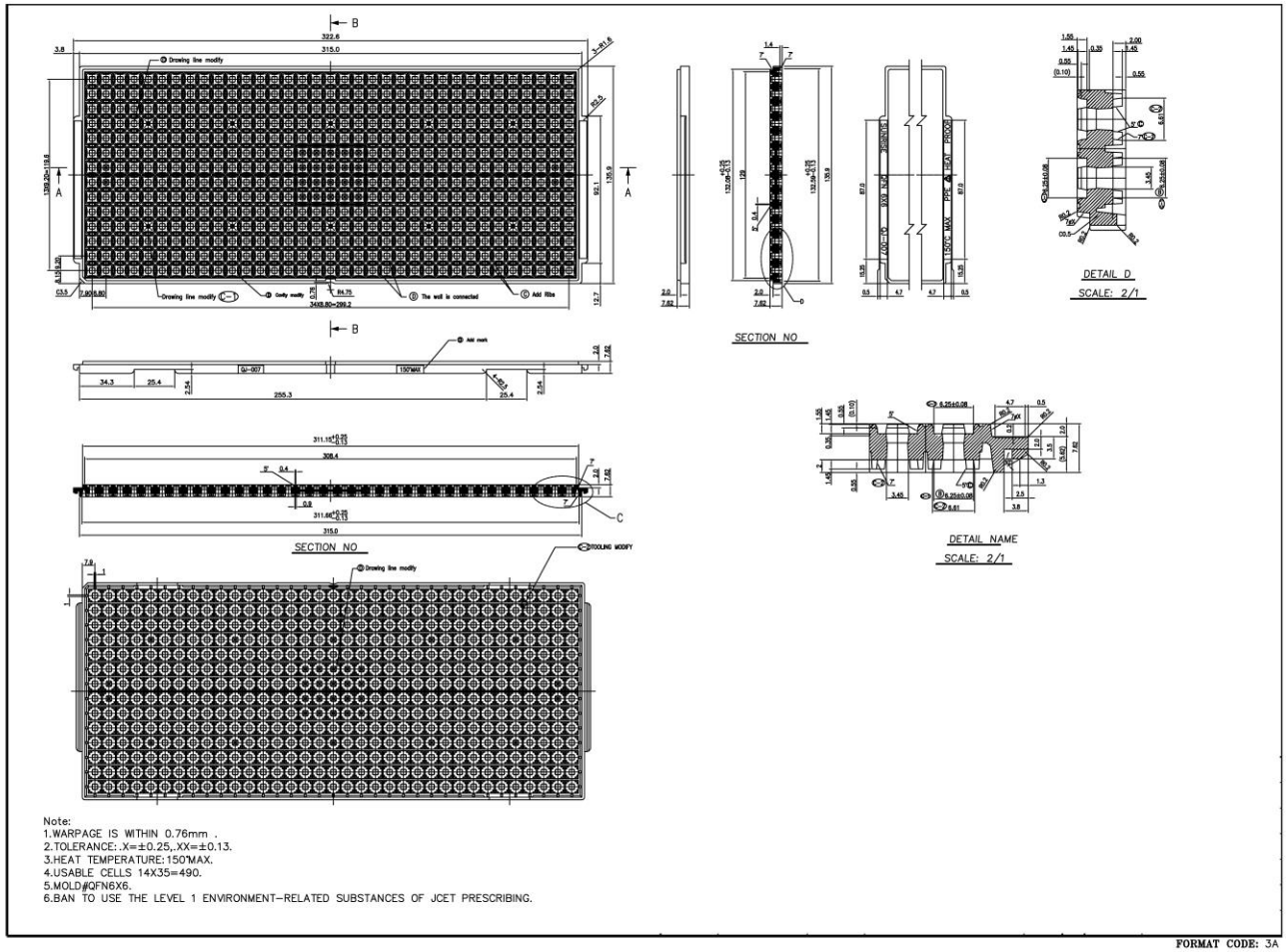



**Figure 9.2.2 Packing Dimensions (JC)**

**Visit our corporate web page at: www.lontiumsemi.com**
**Technical support: support@lontium.com**
**Sales: sales@lontium.com**