# Features

- Enhancement mode
- Very low on-resistance
- VitoMOS® II Technology
- Fast Switching and High efficiency
- 100% Avalanche test

V_{DS}	30	V
$R_{DS(on),TYP}$@ V_{GS}=10 V	4.9	mΩ
$R_{DS(on),TYP}$@ V_{GS}=4.5 V	8	mΩ
$I_{D(Silicon\ Limited)}$	60	A
$I_{D(Package\ Limited)}$	40	A

PDFN3333

Part ID	Package Type	Marking	Packing
VS3620GEMC	PDFN3333	3620GE	5000PCS/Reel

Drain Pin 5-8

Gate Pin4

Source Pin1-3

Maximum ratings, at T_A =25°C, unless otherwise specified

Symbol	Parameter		Rating	Unit
V(BR)DSS	Drain-Source breakdown voltage		30	V
VGS	Gate-Source voltage		±20	V
IS	Diode continuous forward current	T_C = 25°C	60	A
ID	Continuous drain current @VGS=10V (Silicon limited)	T_C = 25°C	60	A
ID	Continuous drain current @VGS=10V (Silicon limited)	T_C = 100°C	38	A
ID	Continuous drain current @VGS=10V (Package limited)	T_C = 25°C	40	A
IDM	Pulse drain current tested ①	T_C = 25°C	240	A
IDSM	Continuous drain current @VGS=10V	T_A = 25°C	21	A
IDSM		T_A = 70°C	17	A
EAS	Avalanche energy, single pulsed ②		20	mJ
PD	Maximum power dissipation	T_C = 25°C	30	W
PD		T_C = 100°C	12	W
PDSM	Maximum power dissipation ③	T_A = 25°C	3.6	W
PDSM		T_A = 70°C	2.3	W
TSTG,TJ	Storage and Junction Temperature Range		-55 to 150	°C

Thermal Characteristics

Symbol	Parameter	Typical	Max	Unit
RθJC	Thermal Resistance, Junction-to-Case	4.2	5	°C/W
RθJA	Thermal Resistance, Junction-to-Ambient	35	42	°C/W

Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T_j=25°C (unless otherwise stated)						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	30	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current(T_j=25℃)	V_{DS}=30V,V_{GS}=0V	--	--	1	μA
	Zero Gate Voltage Drain Current(T_j=125℃)	V_{DS}=30V,V_{GS}=0V	--	--	100	μA
I_{GSS}	Gate-Body Leakage Current	V_{GS}=±20V,V_{DS}=0V	--	--	±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS},I_D=250μA	1.3	1.8	2.4	V
$R_{DS(on)}$	Drain-Source On-State Resistance ④	V_{GS}=10V, I_D=20A	--	4.9	6.4	mΩ
		(T_j=100℃)	--	5.7	--	mΩ
$R_{DS(on)}$	Drain-Source On-State Resistance ④	V_{GS}=4.5V, I_D=10A	--	8	10.5	mΩ
Dynamic Electrical Characteristics @ T_j = 25°C (unless otherwise stated)						
Ciss	Input Capacitance	V_{DS}=15V,V_{GS}=0V, f=1MHz	565	750	1000	pF
Coss	Output Capacitance		415	550	730	pF
Crss	Reverse Transfer Capacitance		55	70	95	pF
Rg	Gate Resistance	f=1MHz	0.2	1.9	5	Ω
Qg(10V)	Total Gate Charge		--	15	20	nC
Qg(4.5V)	Total Gate Charge	V_{DS}=15V,I_D=20A, V_{GS}=10V	--	7.9	10.5	nC
Qgs	Gate-Source Charge		--	2.9	3.9	nC
Qgd	Gate-Drain Charge		--	3.6	5.4	nC
Switching Characteristics						
Td(on)	Turn-on Delay Time	V_{DD}=15V, I_D=20A, R_G=3Ω, V_{GS}=10V	--	5.6	--	ns
Tr	Turn-on Rise Time		--	60	--	ns
Td(off)	Turn-Off Delay Time		--	15	--	ns
Tf	Turn-Off Fall Time		--	9.6	--	ns
Source- Drain Diode Characteristics@ T_j = 25°C (unless otherwise stated)						
V_{SD}	Forward on voltage	I_{SD}=20A,V_{GS}=0V	--	0.9	1.2	V
Trr	Reverse Recovery Time	I_{sd}=20A, V_{GS}=0V di/dt=100A/μs	--	10	20	ns
Qrr	Reverse Recovery Charge		--	1	2	nC

NOTE: ① Single pulse; pulse width ≤ 100μs.

② Limited by T_{Jmax}, starting T_J = 25°C, L = 0.1mH, R_G = 25Ω, I_{AS} = 20A, V_{GS} =10V. Part not recommended for use above this value

③ The power dissipation P_{DSM} is based on $R_{θJA}$ and the maximum allowed junction temperature of 150°C.

④ Pulse width ≤ 380μs; duty cycle≤ 2%.

Typical Characteristics
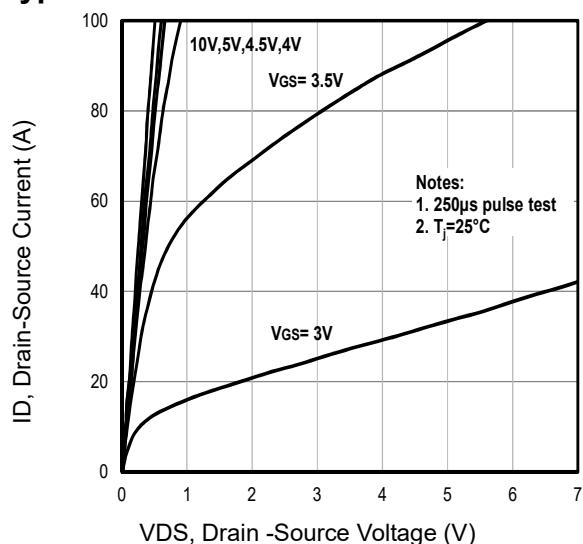
Fig1. Typical Output Characteristics
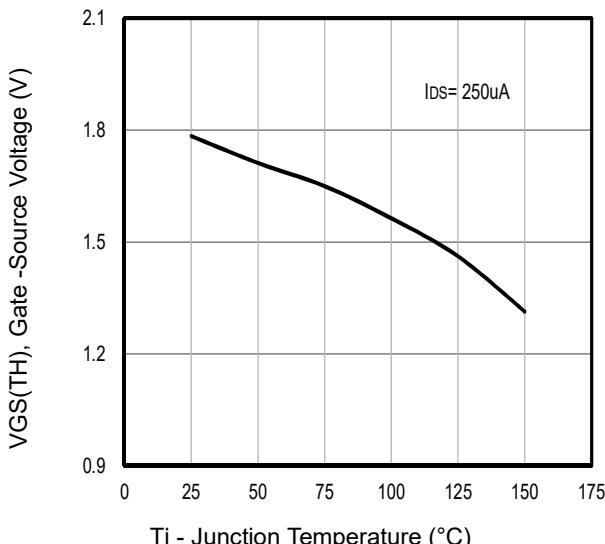
Fig2. $V_{GS(TH)}$ Gate -Source Voltage Vs. Tj
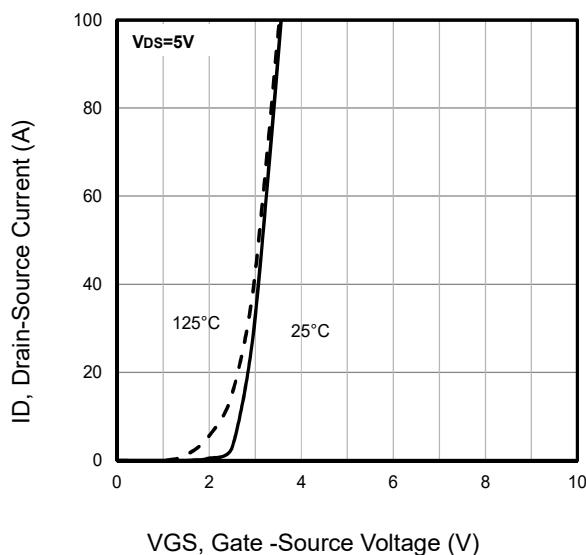
Fig3. Typical Transfer Characteristics
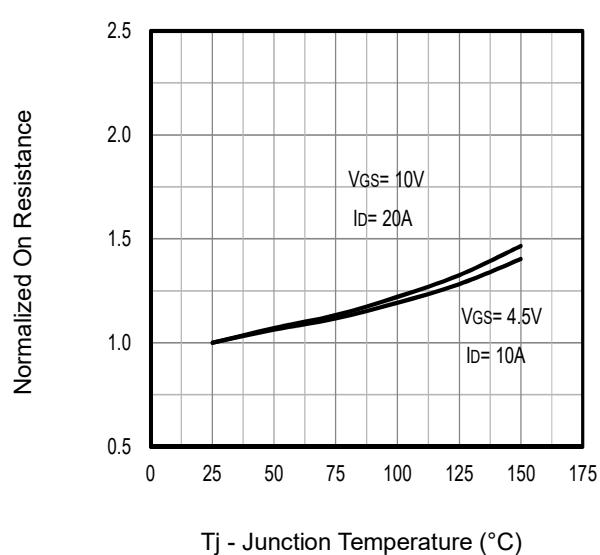
Fig4. Normalized On-Resistance Vs. Tj
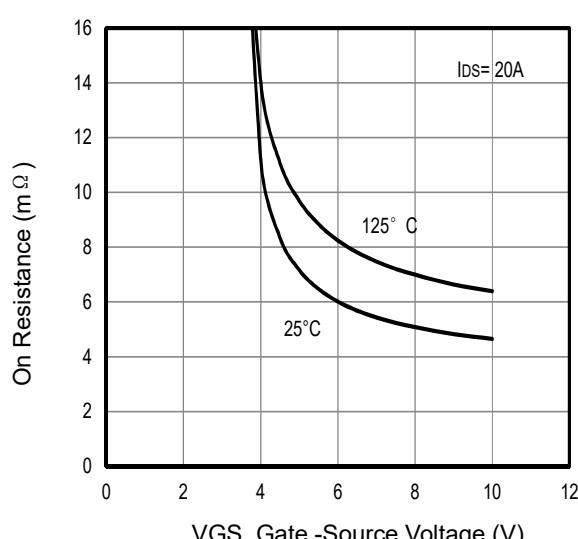
Fig5. On Resistance Vs Gate -Source Voltage
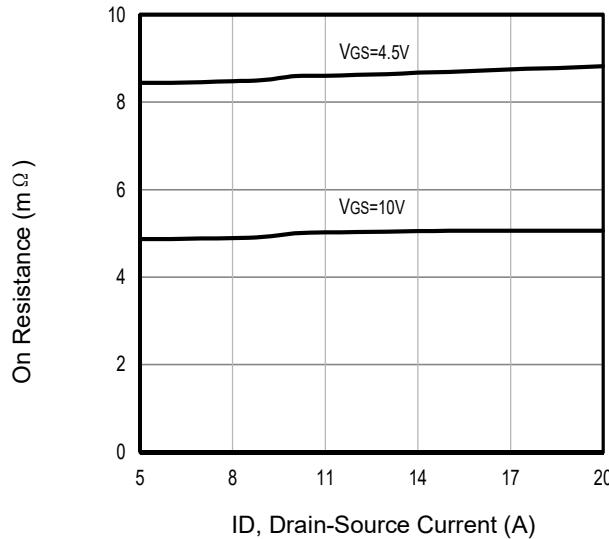
**Fig6.** On Resistance Vs Drain Current and Gate Voltage

Typical Characteristics
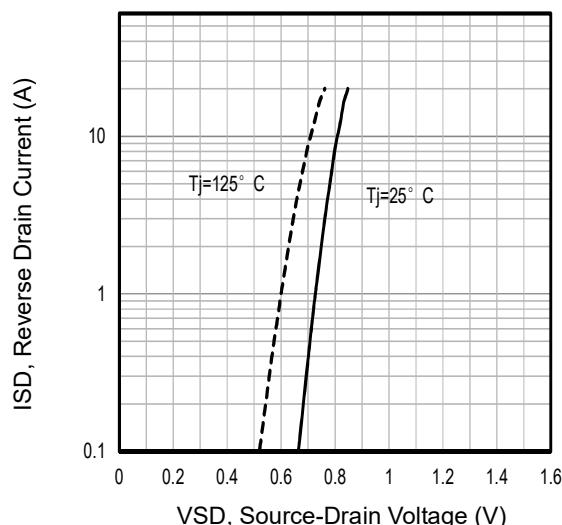
**Fig7.** Typical Source-Drain Diode Forward Voltage
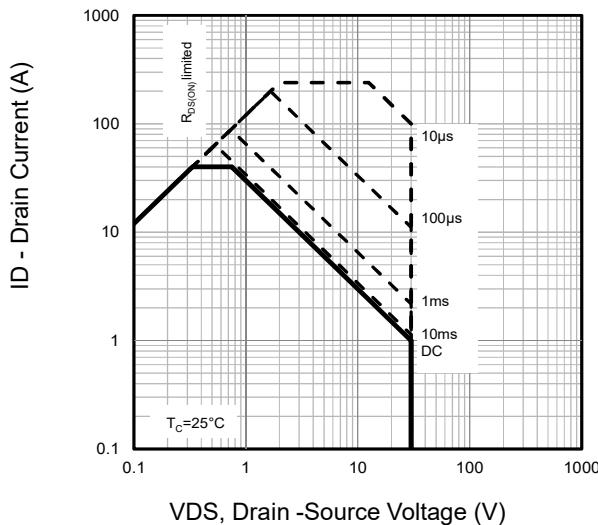
**Fig8.** Maximum Safe Operating Area
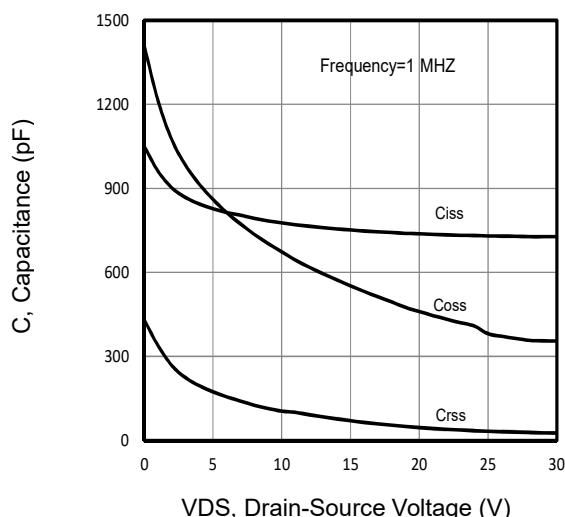
Fig9. Typical Capacitance Vs. Drain-Source Voltage
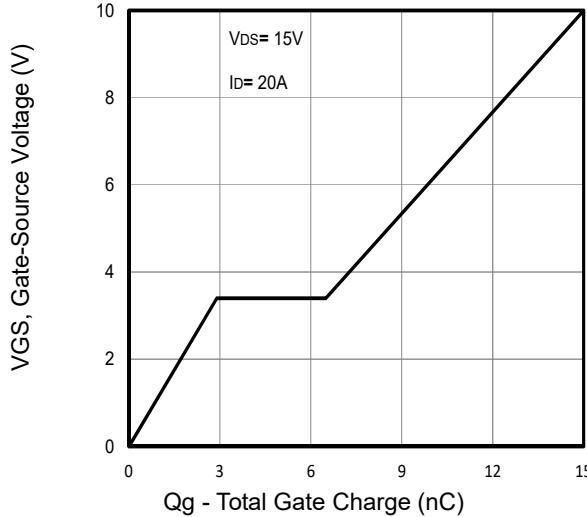
**Fig10.** Typical Gate Charge Vs. Gate-Source Voltage
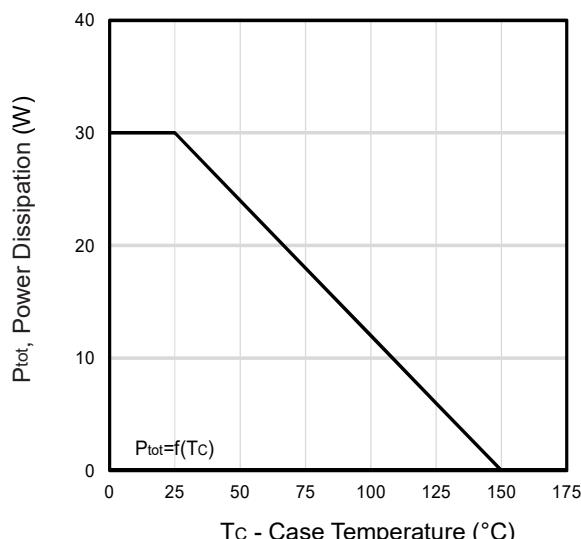

Fig11. Power Dissipation Vs. Case Temperature
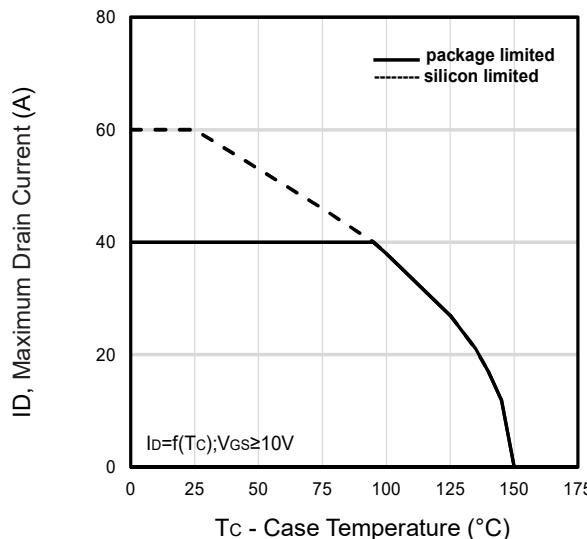
**Fig12.** Maximum Drain Current Vs. Case Temperature

Typical Characteristics
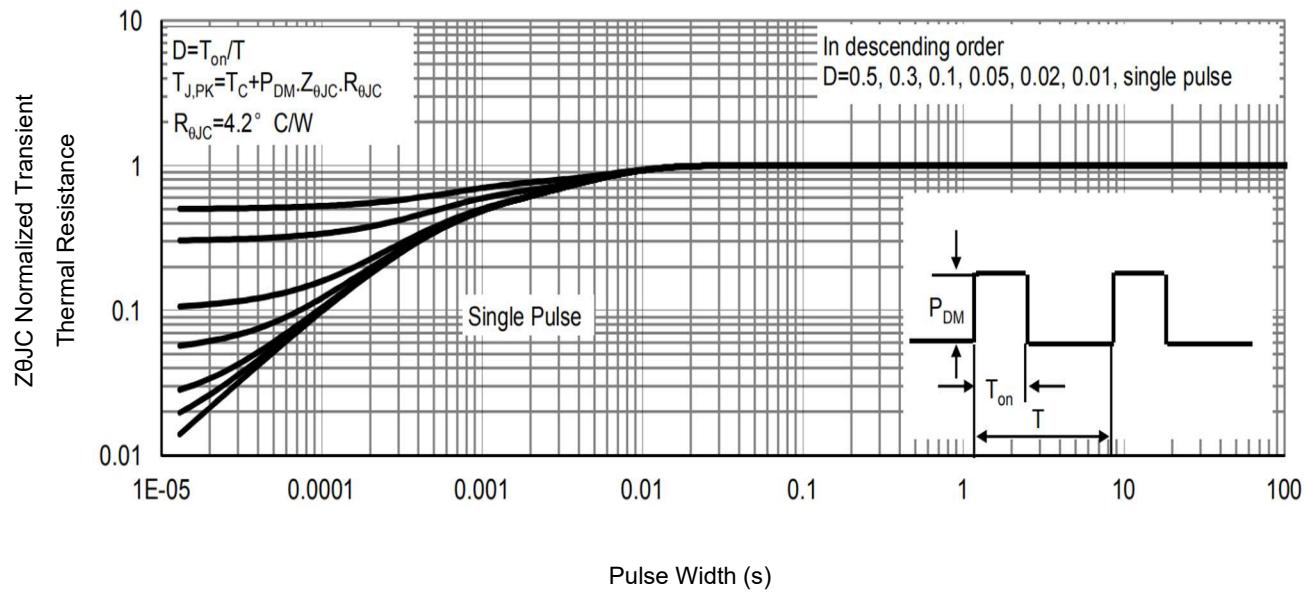
Fig13 . Normalized Maximum Transient Thermal Impedance
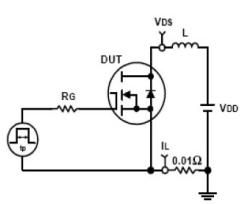
Fig14. Unclamped Inductive Test Circuit and waveforms
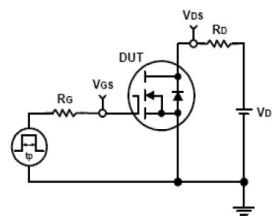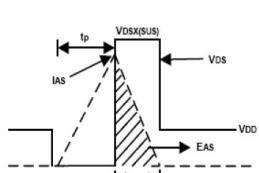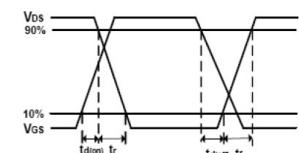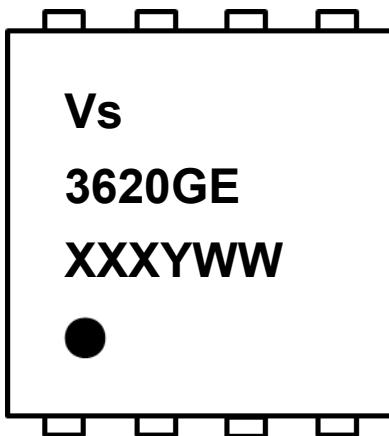
Fig15. Switching Time Test Circuit and waveforms

Marking Information

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   ┌───┴─┴─┴─┴─┴─┴─┴─┴───┐
   │                     │
   │   Vs                │
   │                     │
   │   3620GE            │
   │                     │
   │   XXXYWW            │
   │                     │
   │   ●                 │
   │                     │
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1ˢᵗ line：   Vergiga Code（Vs）

2ⁿᵈ line：   Part Number（3620GE）

3ʳᵈ line：   Date code （XXXYWW）
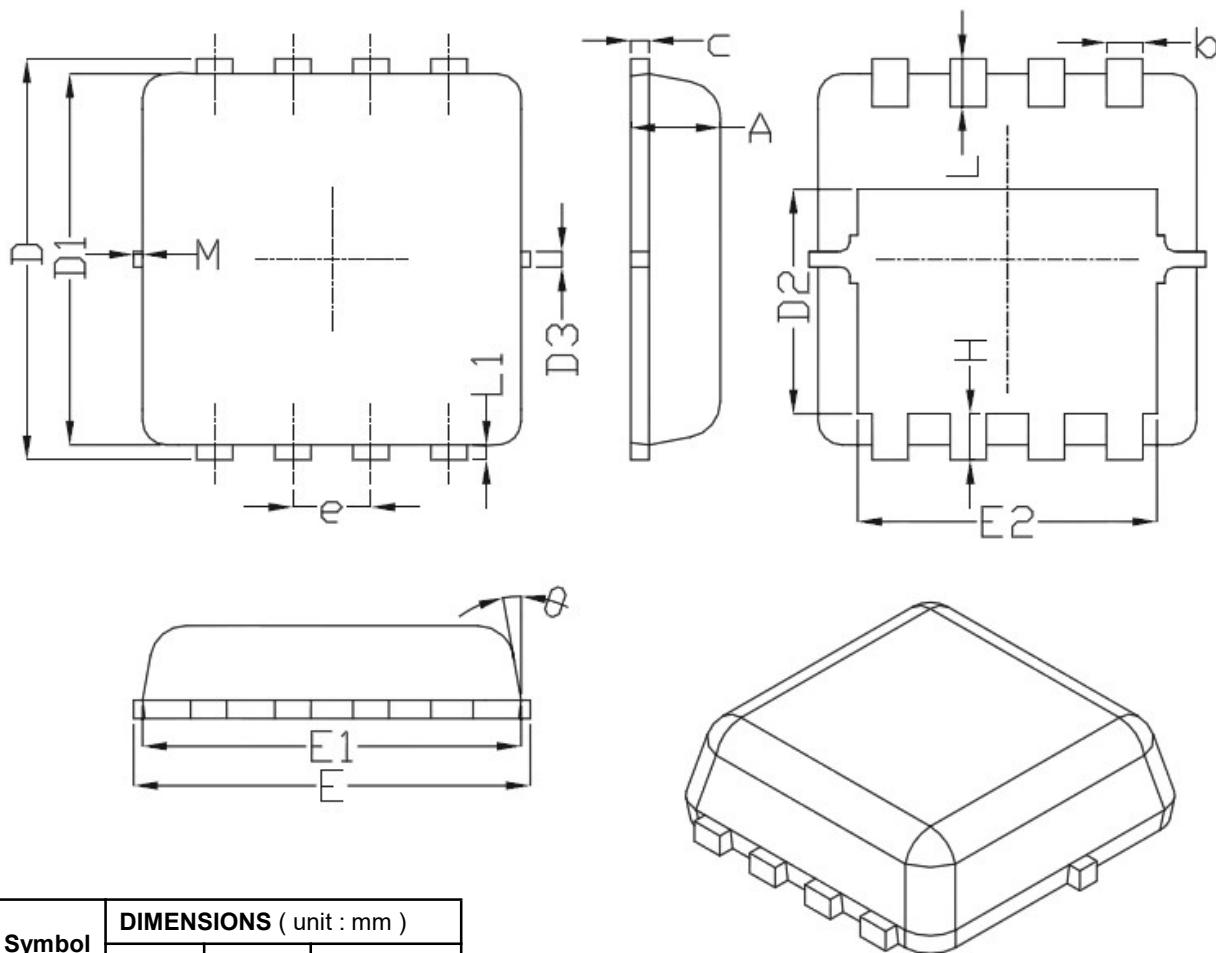
XXX：   Wafer Lot Number Code , code changed with Lot Number

Y：   Year Code , refer to table below

WW：   Week Code (01 to 53)

Code	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T
Year	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030

PDFN3333 Package Outline Data

Symbol	DIMENSIONS (unit : mm)		
	Min	**Typ**	**Max**
A	0.7	0.75	0.8
b	0.25	0.3	0.35
C	0.1	0.15	0.25
D	3.25	3.35	3.45
D1	3	3.1	3.2
D2	1.78	1.88	1.98
D3	--	0.13	--
E	3.2	3.3	3.4
E1	3	3.15	3.2
E2	2.39	2.49	2.59
e	0.65 BSC		
H	0.3	0.39	0.5
L	0.3	0.4	0.5
L1	--	0.13	--
θ	--	10°	12°
M	*	*	0.15
* Not specified			

Notes:

1. Follow JEDEC MO-240 variation CA.

2. Dimensions "D1" and "E1" do NOT include mold flash protrusions or gate burrs.

3. Dimensions "D1" and "E1" include interterminal flash or protrusion. Interterminal flash or protrusion shall not exceed 0.25mm per side.

Customer Service

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